WHAT IS CLAIMED IS:

1. A pipeline accelerator, comprising:

a communication bus; and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit.

2. The pipeline accelerator of claim 1 wherein each of the pipeline units comprises:

a respective memory coupled to the hardwired-pipeline circuit; and

wherein the hardwired-pipeline circuit is operable to,

receive data from the communication bus,

load the data into the memory,

retrieve the data from the memory,

process the retrieved data, and

drive the processed data onto the communication bus.

3. The pipeline accelerator of claim 1 wherein each of the pipeline units comprises:

a respective memory coupled to the hardwired-pipeline circuit; and

wherein the hardwired-pipeline circuit is operable to,

receive data from the communication bus,

process the data,

load the processed data into the memory,

retrieve the processed data from the memory, and

load the retrieved data onto the communication bus.

4. The pipeline accelerator of claim 1 wherein each of the hardwired-pipeline circuits is disposed on a respective field-programmable gate array.

5. The pipeline accelerator of claim 1, further comprising:

a pipeline bus; and

a pipeline-bus interface coupled to the communication bus and to the pipeline bus.

6. The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit; and

a router coupled to each of the branches.

7. The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches;

a pipeline bus; and

a pipeline-bus interface coupled to the router and to the pipeline bus.

8. The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches;

a pipeline bus;

a pipeline-bus interface coupled to the router and to the pipeline bus; and

a secondary bus coupled to the router.

9. The pipeline accelerator of claim 1 wherein:

the communication bus is operable to receive data addressed to one of the pipeline units; and

the one pipeline circuit is operable to accept the data; and

the other pipeline circuits are operable to reject the data.

10. The pipeline accelerator of claim 1, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a router coupled to each of the branches and operable to,

receive data addressed to one of the pipeline units, and

provide the data to the one pipeline unit via the respective branch of the communication bus.

11. A computing machine, comprising:

a processor;

a pipeline bus coupled to the processor; and

a pipeline accelerator comprising,

a communication bus,

a pipeline-bus interface coupled between the pipeline bus and the communication bus, and

a plurality of pipeline units each coupled to the communication bus and each comprising a respective hardwired-pipeline circuit.

12. The computing machine of clam 11 wherein:

the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus;

the pipeline-bus interface is operable to couple the message to the communication bus;

the pipeline units are each operable to analyze the message;

the identified pipeline unit is operable to accept the message; and

the other pipeline circuits are operable to reject the message.

13. The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

wherein the processor is operable to generate a message that identifies one of the pipeline units and to drive the message onto the pipeline bus; and

a router coupled to each of the branches and to the pipeline-bus interface and operable to receive the message from the pipeline-bus interface and to provide the message to the identified pipeline unit.

14. The computing machine of claim 11, further comprising:

wherein the communication bus comprises a plurality of branches, a respective branch coupled to each pipeline unit;

a secondary bus; and

a router coupled to each of the branches, to the pipeline-bus interface, and to the secondary bus.

15. A method, comprising:

sending data to first of a plurality of pipeline units via a communication bus, each pipeline unit including a respective hardwired pipeline; and

processing the data with the first pipeline unit.

16. The method of claim 15 wherein sending the data comprises:

sending the data to a router; and

providing the data to the first pipeline unit with the router via a respective first branch of the communication bus.

17. The method of claim 15 wherein sending the data comprises sending the data to the first pipeline unit with a processor.

18. The method of claim 15 wherein sending the data comprises sending the data to the first pipeline with a second of the plurality of pipeline units.

19. The method of claim 15, further comprising driving the processed data onto the communication bus with the first pipeline unit.

20. The method of claim 15 wherein processing the data with the first pipeline unit comprises:

receiving the data from the communication bus with a hardwired-pipeline circuit,

loading the data into a memory with the hardwired-pipeline circuit,

retrieving the data from the memory with the hardwired-pipeline circuit, and

processing the retrieved data with the hardwired-pipeline circuit.

21. The method of claim 15, further comprising:

wherein processing the data with the first pipeline unit comprises,

receiving the data from the communication bus with a hardwired-pipeline circuit,

processing the received data with the hardwired-pipeline circuit, and

loading the processed data into a memory with the hardwired-pipeline circuit; and

retrieving the processed data from the memory and driving the processed data onto the communication bus with the hardwired-pipeline circuit.

22. The method of clam 15, further comprising:

generating a message that includes the data and that identifies the first pipeline unit as a recipient of the message; and

wherein sending the data to the first pipeline unit comprises determining from the message that the first pipeline is a recipient of the message.